Distributed Scaling Approach of MESFET's and Its Comparison with the Lumped-Element Approach

JYOTI P. MONDAL, MEMBER, IEEE

Abstract—**An appropriate scaling procedure is described for large MESFET cells with experimental verification. A comparison is presented between lumped and distributed modeling approaches. The scalability of elements in the equivalent circuit model of a MESFET is discussed.**

I. Introduction

SCALING LARGE devices from small cells is a common practice. However, if not enough attention is paid to the scalability of an element in the equivalent circuit model, the final device model can differ substantially from the actual measured performance of the original device. This is particularly the case for power amplifiers, where very large cells are used at the output stage to deliver the required amount of power.

In this paper, a systematic approach to scaling up large devices from elementary cells is described. In this approach, the small-signal device performance of large devices is predicted and then matched with the measured data. Throughout this paper discussion is restricted to the linear small-signal analysis only. We will compare two cases, lumped-element and distributed-element. The lumped-element approach is commonly used and lends itself more easily to predicting device performance, depending of course on the device size, the feed structure, and the modeled bandwidth.

At the outset, we must note that there is one assumption in the procedure during scaling: that every gate finger and the associated channel characteristics are identical. For example, in Fig. 1(b), if two in-phase RF signals are applied at the two gate fingers, the RF currents will combine exactly in phase along the width of the drain finger, which is equivalent to having a magnetic wall along the middle of the drain finger and forcing the RF current to flow in only one direction along the width of the drain finger longitudinally. If there is any imbalance between the gate fingers, there will be RF current (odd mode) across the width of the finger; we will not consider this in our modeling of the elementary cell. So all the elements in the equivalent circuit of an elementary cell will correspond strictly to even-mode excitation. In general, this is a fair assumption if the processing of the device is good. Note, even if the gate fingers are exactly identical, there will be some odd-mode current flow across the drain finger, simply because there are manifold distribution effects between any two consecutive gate fingers. However, this effect is negligible, and more concern is placed on the phase delay introduced into the RF signal by the manifold distribution.

In selecting the MESFET devices, it is understood that, even if the processing is standardized, there is some variation in characteristics even among devices on the same

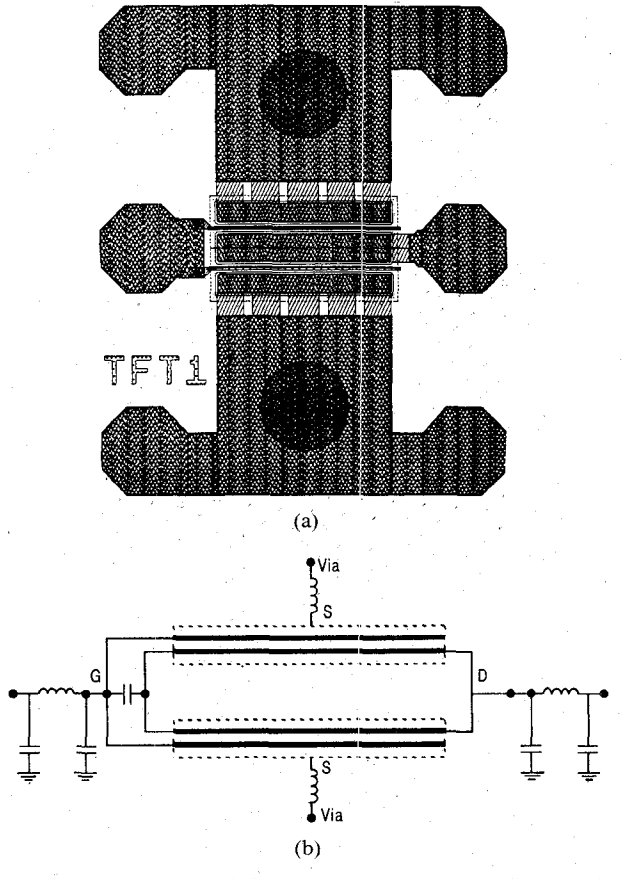


Fig. 1. (a) Elementary cell layout, 400 μm FET (two fingers). (b) A two-finger FET with the drain finger split with a magnetic wall. The bonding and via hole parasitics are also shown.

Manuscript received April 4, 1988; revised February 10, 1989.

The author is with the Sensors and Signal Processing Lab, Honeywell, Inc., Bloomington, MN 55420.

IEEE Log Number 8927784.

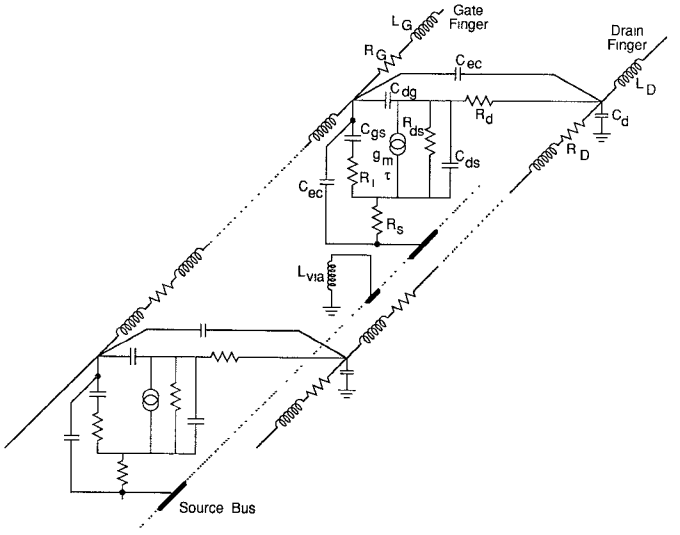


Fig. 2. Distributed modeling of a single-finger FET. The underlying assumption in this sketch is that the current is flowing along the widths of the gate and drain fingers, while on source the current flow is across the width of the finger.

wafer. Devices must be chosen that have minimum variation in channel characteristics and minimum spread in their normalized bias-dependent elements. But these characteristics cannot be determined unless the devices are RF measured and modeled. To avoid such a lengthy process, we chose devices based on simple dc observation: all of the devices were taken from the same reticle and had almost the same normalized $I-V$ characteristics (we set a ± 10 percent limit), and the gate length variation was assumed to be lower from the single reticle than from reticle to reticle. No attempt has been made to relate the dc characteristics to small-signal channel parameters. The dc results are used just as a selection process for the devices which will give small-signal parameters close to one another.

II. Analysis and Measurement

The principle of distributed modeling for MESFET's is thoroughly discussed in the literature [1]. The basic analytical tool to analyze Fig. 2 can be developed from [2, eqs. (1) and (2)], with the proper evaluation of the $[Z]$ and $[Y]$ matrices of the coupled transmission line. We have followed the analytical approach described in [2] and [3], and we have used [4] for determining the starting values of the elements in the $[L]$ matrix of the equivalent circuit model of the FET. These starting values are then optimized to fit the measured S parameters of the device over a number of bias points simultaneously [5]. By combining cold and hot FET data, over a few bias points, it is possible to fix the gate and source parasitic resistances [6], and by further comparing RF-probed data with fixture-mounted data [5], one can also determine the bonding and via hole parasitics. This approach may further be combined with the one described in [7] to refine the elements (with some modification to the source and drain finger capacitances with respect to ground), but in the present case the method in [7] was not used.

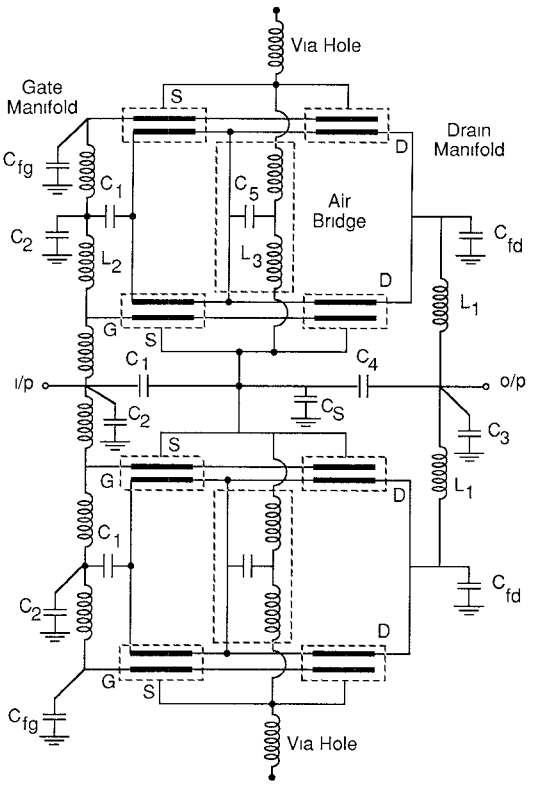
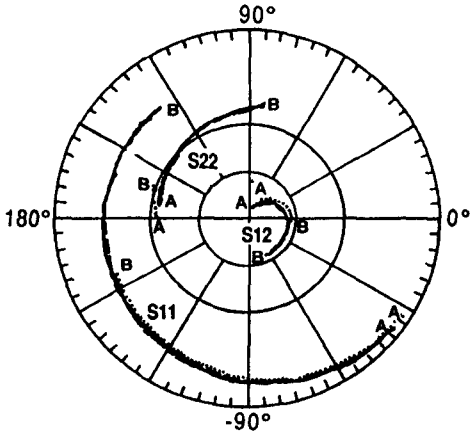


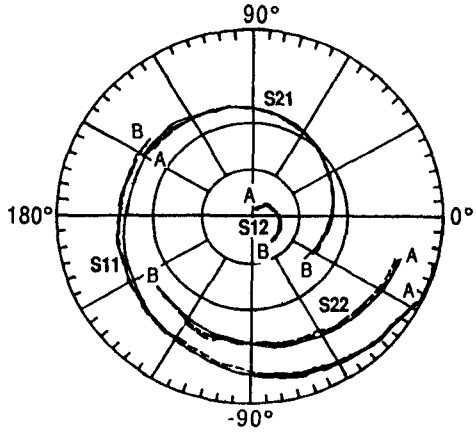
Fig. 3. Semidistributed modeling of a four-finger FET. Each drain finger is divided strictly with a magnetic wall along the middle of its width (even mode only). C_{fg} and C_{fd} are the fringing field capacitances of the gate and drain manifolds, respectively, which are due to open-ended effects of the manifold. On 100 μm GaAs substrate, it is approximately 0.005 pF/100 μm of periphery.

In practice, we have allowed the source and drain series parasitic resistances to vary between hot and cold FET data in order to account for some change in the surface states [8]. This variation does not significantly affect the overall device S parameters. The RF-probed data of an elementary cell on unthinned substrate were compared with the fixture-mounted data of the same cell after thinning the substrate and backside metallization. This comparison gives useful information on bond parasitics and via hole inductance [5]. Once the bonding parasitics are determined, they are maintained within ± 20 percent optimization limits to allow for the variation in manual bonding.

The effects of gate and drain manifold distribution are taken into account by considering them as asymmetrically coupled transmission lines with respect to the device fingers. The coupling capacitances (C_1) between gate manifold and drain finger (a simple case is shown in Fig. 3 for a four-finger FET) have been estimated using the method described in [9]. The same procedure can be applied to C_4 between drain manifold and the source finger. The method has been verified with the theoretical results given in [10]. The manifold distribution effects are treated with lumped elements (Fig. 3), whose values are estimated from coupled transmission lines. Similarly, air bridges are also treated as lumped elements, whose values have been determined by assuming they are microstrip transmission lines.



(a)



(b)

Fig. 4. Sample fitting of lumped and distributed models with fixture de-embedded (bond wires included) S-parameter data for a 400 μm device on polar chart. The fitting is shown for two out of seven bias points, optimized simultaneously. For a cold FET, we also show the RF-probed data for comparison. A: 2 GHz, B: 18 GHz. (a) CF: cold FET, $V_D = 0$ V, $V_G = -2$ V. ---- measured in fixture; ——— lumped model; ——— distributed model; ····· RF-probed data. Radius is "1" for $S11$, $S22$, and $S12$. (b) HF: hot FET, $V_D = 4$ V, $V_G = -3.7$ V. ---- measured in fixture; ——— lumped model; ——— distributed model. Radius is "1" for $S11$, $S22$, and $S12$; "2" for $S21$.

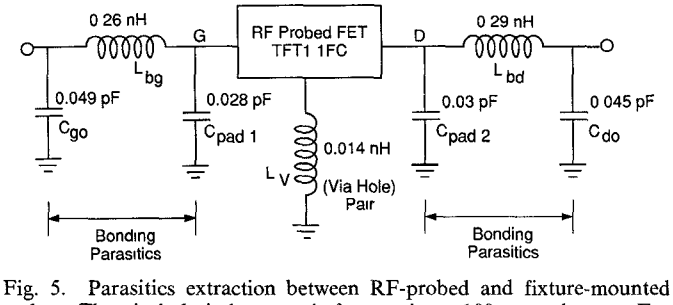


Fig. 5. Parasitics extraction between RF-probed and fixture-mounted data. The via hole inductance is for a pair on 100 μm substrate. For one via hole, it is approximately 0.03 nH.

Figs. 4 and 5 show a sample fitting of the measured S parameters with the lumped and distributed model for a 400 μm device (two fingers, 200 μm each) over a frequency range of 2–18 GHz. The device model has been optimized simultaneously over seven bias points (four cold FET, three hot FET). We have also compared two sets of data,

TABLE I
LUMPED-ELEMENT VALUES AND DISTRIBUTED-ELEMENT VALUES

	BIAS DEPENDENT						BIAS INDEPENDENT								
	C_{dg}	C_{gs}	g_m	R_{ds}	R_i	τ	R_G	L_G	C_{dc}	R_d	R_s	R_D	L_D	C_{ds}*	C_g	L_v
LUMPED	.029	.31	.016	492	5.9	5.9	2.48	.08	.0054	1.2	3.1	NA	.09	.078	NA	.014
DISTRIBUTED	.073	.762	.043	190	1.8	6.2	75	35	.005	.44	1.44	2.3	.41	.203	.024	.013

	BOND PARASITICS					
	C_{pad1}	C_{pad2}	C_{go}	C_{do}	L_{bg}	L_{bd}
LUMPED	.028	.035	.044	.045	.26	.29
DISTRIBUTED	.028	.029	.049	.045	.26	.29

The bias point is HF, as in Fig. 4. Symbols are shown in Figs. 2 and 5. The lumped-element model is not shown separately because it is quite conventional.

All capacitors are in pF, all inductors in nH, all resistors in Ω, g_m is in mho, τ in pS, distributed elements are all per mm, except bond parasitics, τ, and L_v. Distributed elements are all even mode, except bond parasitics and L_v. Even-mode value for L_v is that of a single via hole (~0.03 nH). *C_{ds} assumes one of two values, depending on the bias condition, either hot or cold. This is due to omission of C_{dc} in the model.

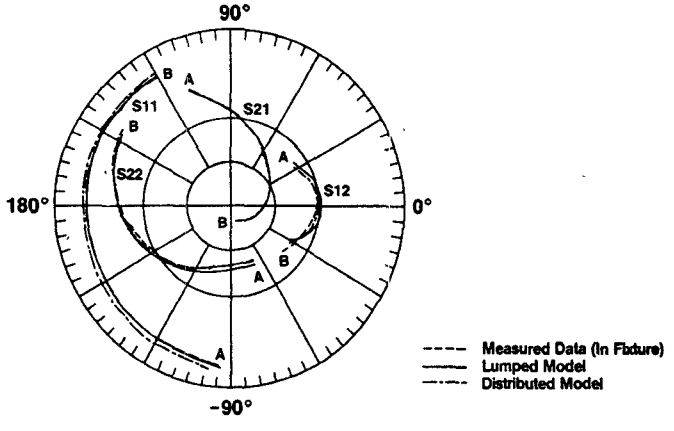


Fig. 6. A sample fitting of a 1600 μm cell (eight fingers) at the same bias point as Fig. 4(b). Both lumped and distributed fittings are shown. We have maintained very close to the same distributed parameters. The lumped parameters can also be scaled for the elementary 400 μm cell, except drain, gate inductances, and C_{ds}. The pad capacitances and the via hole inductances are also different. For symbols, refer to Fig. 2, Fig. 5, and Fig. 3. A: 2 GHz, B: 18 GHz. Radius is "1" for $S11$ and $S22$; "4" for $S21$; and "0.2" for $S12$.

RF-probed and fixture-mounted, at all seven bias points simultaneously. We show the fitting only at two bias points. Fig. 5 shows the extraction of parasitics due to via holes and the bond wires. Note that both the distributed and lumped-element models can predict the performance very well for this device over the frequency range 2–18 GHz (Table I).

Fig. 6 shows the lumped- and distributed-element fitting of a 1600 μm device (eight fingers). The normalized channel current is the same as one of the bias points (HF) for the device in Figs. 4 and 5. The scaled-up lumped elements from the elementary cells (400 μm) are quite close to most of the optimized lumped elements for 1600 μm (Table II),

TABLE II
LUMPED AND DISTRIBUTED VALUES OF A 1600 μm CELL

	BIAS DEPENDENT						BIAS INDEPENDENT								
	C_{dg}	C_{gs}	g_m	R_{ds}	R_i	τ	R_G	L_G	C_{ec}	R_d	R_s	R_D	L_D	C_{ds}	C_d	L_v^*
LUMPED	.115	1.19	.066	101	1.57	6.5	.62	.013	.016	.4	1.1	NA	.021	.36	NA	.026
DISTRIBUTED	.070	.82	.045	178	1.95	6.2	74	.35	.005	.41	1.51	2.1	.4	.186	.024	.016

	BOND PARASITICS					
	C_{pad1}	$C_{pad2}^\dagger$	C_{go}	C_{do}	L_{bg}	L_{bd}
LUMPED	.036	.078	.04	.049	.23	.21
DISTRIBUTED	.030	.031	.04	.049	.23	.21

MANIFOLD + AIR-BRIDGE PARASITICS (FIG. 3)							
C_1	C_2	C_3	C_4	C_5	L_1	L_2	L_3
.0021	.0038	.0065	.0033	.006	.011	.008	.0012

The cell has eight fingers and the bias point is the same as in Fig. 4.
*L_v is modified by air-bridge inductance in the lumped-element model. Distributed parameters are all per mm, except bond parasitics, τ, and L_v. Distributed parameters are all even mode, except bond parasitics and L_v. Even-mode value for L_v is that of a single via hole, which is 0.032 nH in this case.
†C_{pad2} is modified by drain finger capacitance and drain manifold capacitance in the lumped-element model.
Gates are approximately 45 μm apart. Air bridge is treated as microstrip lines 40 μm wide and 2.5 μm high with air dielectric.

with the exception of the gate and drain inductances (which tend to absorb the manifold inductances), the pad capacitances (which will absorb the manifold capacitances and drain finger capacitances), and the effective via hole inductance (which tends to increase because of air bridge inductance). One more element, C_{ds}, may not scale directly, depending on the air bridge capacitance with respect to the drain finger. In the present case, the contribution is negligible. For scaling the series elements (R_G, L_G, L_D, and R_D) in the lumped-element model, the following formula has been used:

$$\frac{X_2}{X_1} = \left(\frac{W_2}{W_1}\right) \cdot \left(\frac{N_1}{N_2}\right)^2 \tag{1}$$

where $W_{1,2}$ denote the total gate widths, $N_{1,2}$ are the total numbers of gate fingers, and $X_{1,2}$ are the corresponding series elements (R_G, L_G, L_D, or R_D). On the other hand, in distributed modeling, we maintain the same normalized distributed parameters along with the pad capacitances.

In distributed modeling of bigger cells, we first hold the $[Z]$ and $[Y]$ matrix/unit length (determined from elementary cell measurements) constant and optimize for the manifold and air bridge parasitics simultaneously over five bias points. Then we let the bias-dependent elements in the $[Y]$ matrix vary by approximately ± 10 percent to obtain an overall good fit for all the bias points. This is necessary to account for device-to-device variations, especially for bigger cells, where there is an averaging-out effect because all the fingers may not be identical. One reason for modeling the manifold parasitics in lumped form is that the junction effects are easily absorbed in the lumped elements.

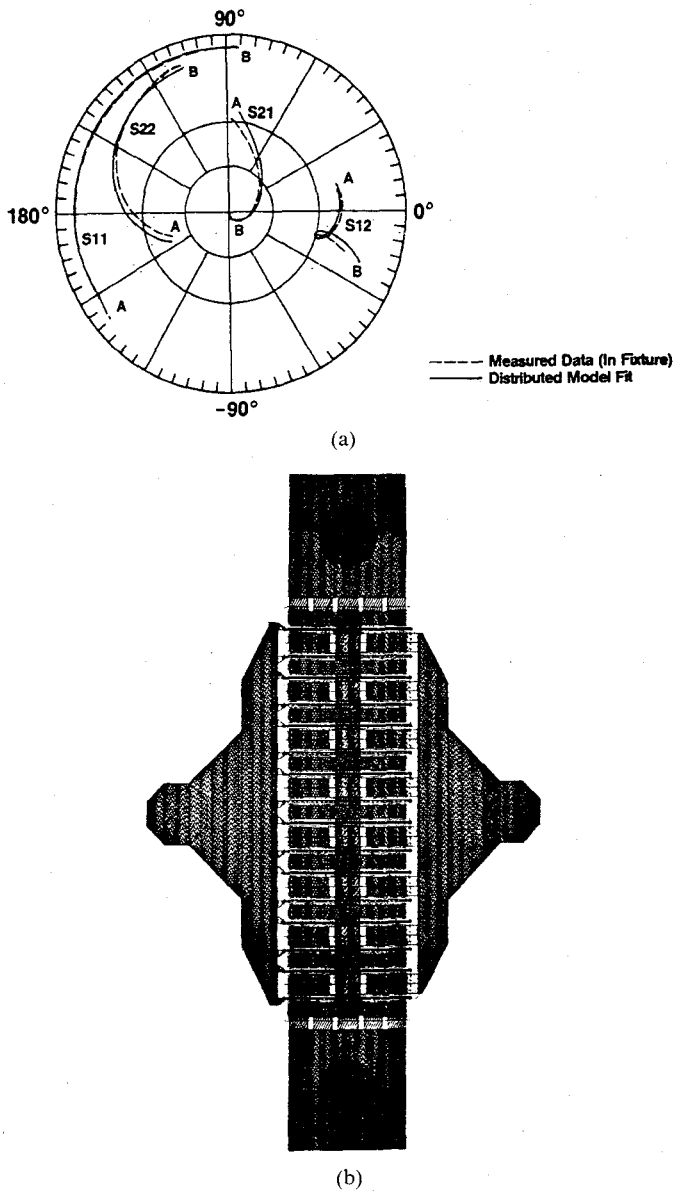


Fig. 7. (a) A sample fitting of a 3200 μm cell (16 fingers) with a distributed model. The scaled-up lumped element model could not be fitted with the measured S parameters as well as the distributed model. Radius is "1" for $S11$ and $S22$; "4" for $S21$; and "0.1" for $S12$. A: 2 GHz, B: 18 GHz. (b) Cell layout for a 3200 μm cell. A slight misfit in (a) seems to be due to a somewhat different feed structure in this cell.

Fig. 7 shows another device: 3200 μm total gate periphery, 16 fingers, 200 μm each. This FET is not as easily modeled over 2–18 GHz with scaled-up lumped elements, but with the distributed model, keeping approximately the same normalized distributed parameters as in Table I, we were able to obtain a much better prediction. There is a slight misfit between the distributed model and the measured S parameters (Fig. 6(a)). It is even more pronounced in $S21$, showing that the average value of R_{ds} and/or g_m may be slightly beyond the range of variation we have given (± 10 percent) for the bias-dependent elements. The

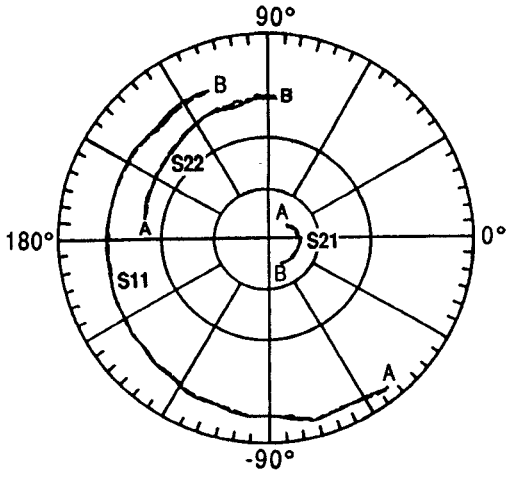


Fig. 8. A sample distributed model fit to the in-fixture data of a 600 μm device (two fingers) at a cold FET bias point, $V_D = 0$ V, $V_G = -2$ V. A: 2 GHz, B: 18 GHz. Equivalent circuit model is different from that of hot FET. It is not shown here. The model for $[Y]$ matrix is similar to that given in [15]. Radius is "1" for $S11$, $S22$, and $S21$. ---- measured in fixture; ——— distributed model.

misfit in $S11/S22$ may be caused by a slightly different feed structure for this cell (Fig. 7(b)).

The same unit finger gate width (200 μm) was used for the devices in Figs. 4–7. Fig. 8 shows a distributed model fit for a 600 μm (300 μm unit finger width) device at a cold FET bias point. This is one of the seven bias points optimized simultaneously. The bias points are the same as in device reported in Figs. 4 and 5. Once again the distributed parameters are very much the same as in Fig. 4(a).

The reason for keeping the same unit finger width for the devices in Figs. 4–7 is to observe the effects of manifold distribution and air-bridge parasitics. In our analysis, the effect of skin resistance and self-internal inductance have not been taken into account. Over the frequency range being considered, the changes in the $[R]$ and $[L]$ matrices of the gate and drain lines are negligible.

Finally, it is possible to simulate the distributed response of a MESFET by segmentation of the FET fingers, as shown in Fig. 9. For a FET, there are two propagation modes (determined by $[Y]$ and $[Z]$ matrices only); the segment Δl should be much smaller than the smaller of the two propagating wavelengths. Fig. 9 is derived by a fitting process, in which the factor $(1/3)$ for the $[Z]$ matrix was optimized in order to obtain a good fit between n cascaded sections and the exact solution for the coupled line structure having length $n\Delta l$. The four nodes of the segment Δl are denoted as (1), (2), (3), and (4) in Fig. 9. This method of simulating the distributed response is quite amenable to SUPER-COMPACT format, because all the elements are known and can be simulated in SUPER-COMPACT.

It takes approximately 2–3 hours of CPU time on the VAX 8600 for seven-bias-point optimization in distributed form with double precision, so the optimization can be carried out overnight in batch jobs. The CPU time may be reduced with a better algorithm and proper starting values.

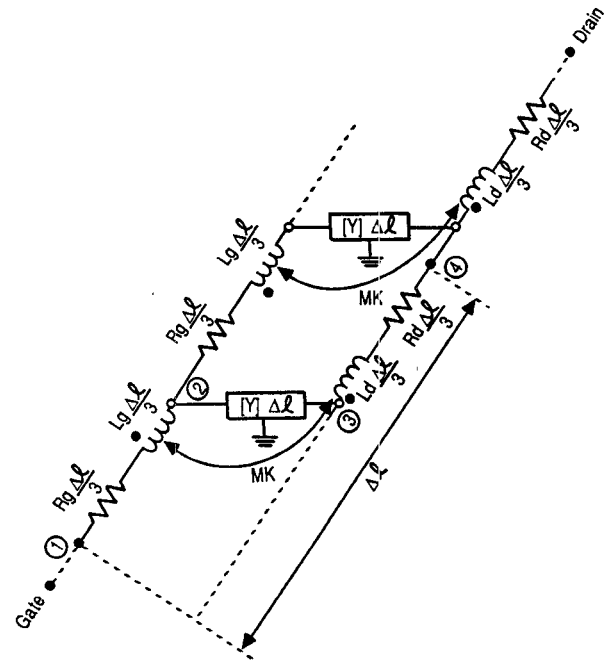


Fig. 9. Segmentation of a single-fingered FET; the figure is derived by a fitting process in which the factor for the $[Z]$ matrix is optimized to get a good fit with the exact solution of the coupled line structure. Δl is a segment along the width of the FET and should be much smaller than the propagation wavelengths along the gate and drain fingers.

The resistances R_s, R_d, and R_G have first been estimated by the experimental procedures described in [11] and [12]. They are then optimized around these values simultaneously over all the bias points.

III. Conclusion

It has been shown that, with proper methodology (dependent on the device structure), it is possible to theoretically predict larger cell performance by scaling it from elementary cells. How well the device performance can be predicted is dependent on processing uniformity. Since this device nonuniformity is always present, it is suggested that a few elementary cells (with two fingers) be put in every reticle as test element groups (TEG's). The measurement on these elementary cells will reflect the variation in the bias-dependent elements (which, in turn, reflects the process or material variation). These variations are then used to make a sensitivity analysis, keeping the same fundamental structure. This will bypass using large cells in TEG's, which not only consume a lot of real estate but are very difficult to measure. We also show that, with proper de-embedding and optimization techniques, it is possible to estimate quite a few parasitic elements. The RF-probed and fixture–de-embedded data are properly correlated simultaneously over quite a few bias points to determine the bond wire and via hole related parasitics.

The entire procedure (scaling and experimental verification) should be carried out at least once; once the cell structures are well established, it is only required to make measurements on the elementary cells.

In a very recent article [13], one way has been described to separate out pad capacitances from C_{gs} and C_{ds} by

taking measurements with different pad dimensions. The same goal can be achieved by comparing RF-probed data (on unthinned substrate) with fixture-mounted data of an elementary cell simultaneously at quite a few bias points (both cold and hot FET's), $-C_{gs}$ being a strong function of gate voltage and C_{ds} being a strong function of drain voltage between cold and hot FET's. In this way device-to-device variation can be minimized. The values found for the pad capacitances, C_{pad1} and C_{pad2}, in our case compare very well with the experimentally determined values for isolated pads on 100 μm GaAs substrate [14].

A good way to minimize the effect of air-bridge capacitance on C_{ds} during scaling is to put the air bridge in the two-fingered cell itself and repeat the structure.

We have modeled the manifold distributions (drain and gate) as lumped low-pass structure in order to absorb the discontinuities (mostly T junctions) which are very closely spaced. The other alternative—electromagnetic simulation—has been avoided here. The same is true for air bridges. By doing this, one need not lose any accuracy; the cutoff frequency associated with such structures is quite high compared with the maximum measurement frequency. Each resonator section in air bridge (Fig. 3) has a cutoff frequency $1/\sqrt{L_3C_5/2}$; that of the gate manifold is $1/\sqrt{L_2(C_2/2+2C_1)}$ and that of the drain manifold is $1/\sqrt{L_1(C_3/2+2C_4)}$ (the higher order modes will appear at frequencies much lower than these cutoff frequencies).

Appendix

The series elements R_G, L_G, L_D, and R_D are related in the lumped and distributed cases by the following expressions:

$$X_{\text{lumped}} \simeq \frac{1}{3} \cdot \left(\frac{X_{\text{distributed}} \cdot W}{n} \right)$$

where

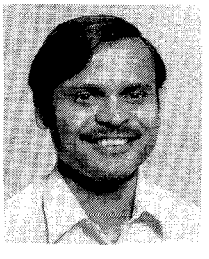
$X_{\text{lumped}} = R_G$, L_G, L_D, or R_D in lumped case,
$X_{\text{distributed}} = R_G$, L_G, L_D, or R_D in distributed case/ mm,
W = unit finger width in mm,
n = number of fingers.

Acknowledgment

The author wishes to thank L. S. Rider for his support of this work. The author also extends his thanks to A. Thatcher for mounting and bonding chips during her tight schedule. B. Craig and B. Cleaveland have helped improve the clarity of this paper.

References

[1] W. Heinrich, "Distributed equivalent circuit model or traveling-wave FET design," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 487–491, May 1987.
[2] V. K. Tripathi, "Asymmetric coupled transmission lines in an inhomogeneous medium," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, pp. 734–739, Sept. 1975.
[3] J. P. Mondal, "An experimental verification of a simple distributed model of MIM capacitors for MMIC applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 403–407, Apr. 1987.
[4] K. C. Gupta *et al.*, *Computer Aided Design of Microwave Circuits.* Dedham, MA: Artech House, 1981, p. 281.
[5] J. P. Mondal and C. H. Chen, "Propagation constant determination in microwave fixture de-embedding procedure," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 706–714, Apr. 1988.
[6] W. R. Curtice and R. L. Camisa, "Self-consistent GaAs FET models for amplifier design and device diagnostics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 1573–1578, Dec. 1984.
[7] R. A. Larue *et al.*, "A 12 dB high-gain monolithic distributed amplifier," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 2073–2078, Dec. 1986.
[8] S. Chaudhuri and M. B. Das, "An investigation of MESFET end resistance using a distributed diode/resistance model," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 2262–2268, Nov. 1985.
[9] P. K. Ikalainen and A. L. Matthaei, "Wide-band forward-coupling microstrip hybrids with high directivity," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 719–725, Aug. 1987.
[10] R. H. Jansen, "Fast accurate hybridge mode computation of non-symmetrical coupled microstrip lines," in *Proc. 7th European Microwave Conf.*, 1977, pp. 135–139.
[11] A. Materka and T. Kacprzuk, "Computer calculation of large signal GaAs FET amplifier characteristics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 129–135, Feb. 1985.
[12] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *Bell Syst. Tech. J.*, vol. 58, no. 3, pp. 771–797, Mar. 1979.
[13] E. W. Strid, "Extracting more accurate FET equivalent circuits," *Monolithic Technol.*, pp. 3–7, Oct. 1987.
[14] A. Higashisaka and F. Hasegawa, "Estimation of fringing capacitance of electrodes on S.I. GaAs substrate," *Electron. Lett.*, no. 11, pp. 441–412, 22 May 1980.
[15] L. Chainulu Upadhyayula *et al.*, "Passive GaAs FET switch models and their application in phase shifters," in *1987 IEEE MTT-S Dig., Int. Microwave Symp.*, pp. 903–906.



Jyoti P. Mondal (S'82–M'84) was born in Calcutta, India. He received the bachelor of technology degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, in 1977 and the M.S. and Ph.D. degrees, both in electrical engineering, from Carnegie Mellon University, Pittsburgh, PA, in 1981 and 1984, respectively.

From 1977 to 1980 he worked with Bharat Electronics Limited, Ghaziabad, India, as an R&D Engineer, developing bipolar power and low-noise amplifier circuits in the *L*-band. His project and thesis work for the M.S. and Ph.D. degrees included variable-gain amplifiers and monolithic phase shifters for *S*-band applications. He was with General Electric Company, Electronics Lab, Syracuse, NY, from December 1984 to August 1988. Since then he has been working with the millimeter-wave group at the Sensors and Signal Processing Lab, Honeywell, Bloomington, MN 55420. His present activities are mainly in the microwave monolithic circuit area and involve RF circuits, device physics, and measurement techniques.